

# EUROPEAN PATENT OFFICE

## Patent Abstracts of Japan

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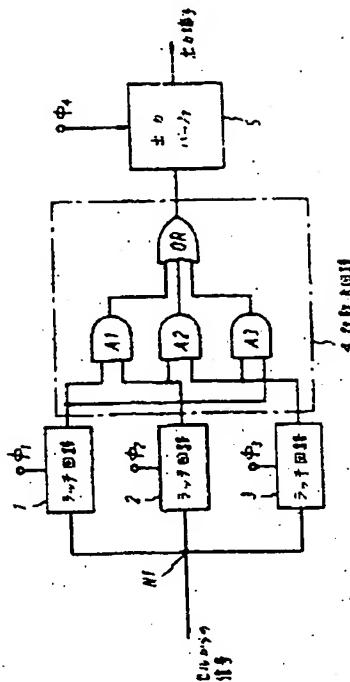
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TITLE : MEMORY READ SYSTEM



ABSTRACT : PURPOSE: To prevent erroneous read due to an electric noise without reducing the bit density by reading information from the same cell plural times continuously and comparing these information to determine output information.

CONSTITUTION: Information read to a node N1 is taken into a latch circuit 1 by a control clock  $\varphi_1$  and is latched. Information is read again from the same cell, and read information is latched in a latch circuit 2 by a control clock  $\varphi_2$ , and information read from the same cell is latched in a latch circuit 3 by a control clock  $\varphi_3$  similarly. Three pieces of latched information are subjected to majority decision by a majority decision circuit 4, and the result is read out to the external through an output buffer 5. The majority decision circuit 4 consists of 3 AND circuits A1~A3 and one OR circuit OR and outputs the same information as information inputted to the majority of the first ~ third input terminals.

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